

A novel thermorefectance-based method for in-situ die attach thermal conductivity assessment of packaged devices

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High-power density, high-efficiency electronic devices are increasingly demanded in a variety of applications, e.g. space application. High power density requires effective thermal management at the packaging level to ensure that operating temperatures remain in a safe operating range, avoiding early device failures. The die attach (bond layer between die and flange) has been a thermal bottleneck, relying on relatively low thermal conductivity eutectic solders. Advanced high thermal conductivity die attach materials, including sintered silver and silver epoxies, are being developed to address this. However, the thermal conductivity of these new materials is typically assessed in their bulk form; the bulk thermal conductivity may not be representative of the lower actual “effective” thermal conductivity in a real application, which is also affected by interfaces and voids. In this paper, frequency domain thermorefectance has been adapted to operate at low frequency, with depth sensitivity to measure the thermal conductivity of a die attach layer sandwiched between a die and flange.

High-power GaN-on-SiC RF transistors, used in communications and radar applications, have tremendously high areal power dissipation densities, and are potentially one of the most difficult thermal management challenges. Many die attach materials have been developed, for example, gold-tin (Au-Sn), gold-silicon (Au-Si), nanoscale silver sintering [1] and silver loaded epoxies. One of the important properties of a die attach is its thermal conductivity since it affects the overall thermal resistance of the packaged device. So far, to determine the thermal conductivity of the die attach materials, steady-state or laser flash (LFA) methods have been used on bulk stand-alone samples [2], i.e., not necessary representative of real applications. A technique is needed to measure the die attach layer in-situ, including any non-idealities such as voids or interfacial thermal resistances between dissimilar layered materials.

Frequency domain thermorefectance (FDTR) would be ideal in principle because the probing depth can be selected by changing the modulation frequency. However, existing FDTR equipment is designed for high frequency measurements (10’s kHz to MHz) and uses relatively low lasers powers, meaning that is only sensitive to nm- μ m depths [3]– ideal for thin film analysis but it cannot “see” the die attach layer under the transistor die. In this work, the FDTR modulation frequency has been greatly reduced, extending the use of this technique to packaged devices with layer thickness of 10’s μ m to millimeters [4].

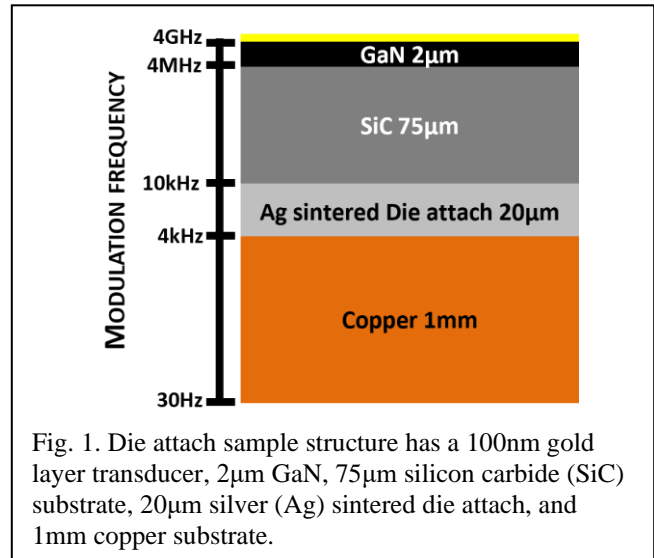


Fig. 1. Die attach sample structure has a 100nm gold layer transducer, 2 μ m GaN, 75 μ m silicon carbide (SiC) substrate, 20 μ m silver (Ag) sintered die attach, and 1mm copper substrate.

To demonstrate low-frequency FDTR, the die attach thermal properties of packaged GaN-on-SiC die are measured directly, in-situ, illustrating the effect of voids. Note that in-situ die attach total thermal resistance has been successfully measured using frequency-domain transient electrical heating/thermometry [5]. However, this technique requires fabrication of electrical heaters and thermal sensors, compared to the presented low-frequency FDTR technique

which requires only minimal sample preparation. Low-frequency FDTR is also applicable to other materials and technologies.

FDTR is an optical pump-probe configuration which in our case uses a frequency-modulated high power pump laser (450nm) to periodically heat a sample and uses a 520nm probe laser to monitor the surface temperature change, ΔT . The relative change in the transducer reflectivity ΔR is proportional to the change in surface temperature ($\Delta R/R \propto \Delta T$). The modulation frequency (f) determines the thermal penetration depth. The new FDTR instrument is designed to work from ~ 10 Hz up to 10kHz, extending the probing depth to mm's. Low modulation frequency, large pump spot size, combined with a high pump laser power, gives a highly selective depth sensitivity to individual layers within a packaged device [4]. FDTR measures the phase shift of the reflective probe laser in response to the pump laser as a function of frequency. The phase shift is measured as a function of the modulation frequency, which is then fitted using an analytical multilayer axisymmetric heat diffusion model to obtain the thermal properties of each layer; these can include the specific heat capacities and thermal conductivities. Error analysis was made using the co-variance matrix method of Ref. [6]. A pump and probe spot size of 520 μ m and 30 μ m have been used, respectively. The FDTR instrument was initially calibrated using a pure silicon sample with known thermal properties and the thermal conductivity accuracy verified for a range of uniform bulk materials with thermal conductivities ranging from 30-1000 W/m \cdot K [4].

Two GaN-on-SiC transistor dies were mounted onto a copper flange using silver-based die attach products from different vendors, but otherwise having the same structure, which is presented in **Error! Reference source not found.**; note that this measurement required optical access to the top surface which can be gained by de-lidding. Both samples were measured using FDTR from 100Hz to 10kHz (~ 0.8 mm depth). In this case, the thermal properties of all the layers are known, apart from the thermal conductivity of the die attach layer, which is the parameter of interest. We consider the *effective* thermal conductivity of the die attach layer, which is a lumped value combining the thermal conductivity and potential the thermal boundary resistances at the SiC/die attach and die attach/copper interfaces.

The results are presented in Fig. 2 along with the best fit analytical model. The known material properties used in the thermal model, for GaN, SiC and copper are listed in Table I. An effective die attach thermal conductivity of 72 ± 5 W/m \cdot K was determined for Sample 1, which is lower than manufacturers specifications (100-200W/m \cdot K reported by different vendors). However, data sheet values are typical measured on bulk materials using LFA. Measurements such as LFA neglect the thermal boundary resistance at the interfaces and the potential formation of voids close to the interfaces [4]-[5], in the real sandwiched structures, which as shown in Fig. 1. This highlights the importance of measuring the actual in-situ die attach effective thermal conductivity.

It is noteworthy that sensitivity to the silver sintered die attach thermal conductivity peaks at ~ 4 kHz, for Sample 1. Up to 6kHz, the measured data agrees very well with the fitted analytical model, with minor differences at higher frequencies. Regarding Sample 2, the reflected phase deviates from the response of Sample 1 above 1kHz. The decreasing phase shift at higher frequency implies that thermal resistance of die attach layer of Sample 2 is very high; to reproduce this trend in the model, the die must be thermally insulated from the copper heatsink. To investigate the physical differences which cause the different results for samples 1 and 2, X-ray transmission imaging has been performed for both samples (presented in the inset of **Error! Reference source not found.** Fig. 2). In Sample 2, the Xray images show a presence of large voids ($\sim 60\mu$ m width) and low-density areas in the die attach layer. In contrast, the die attach layer of Sample 1 is

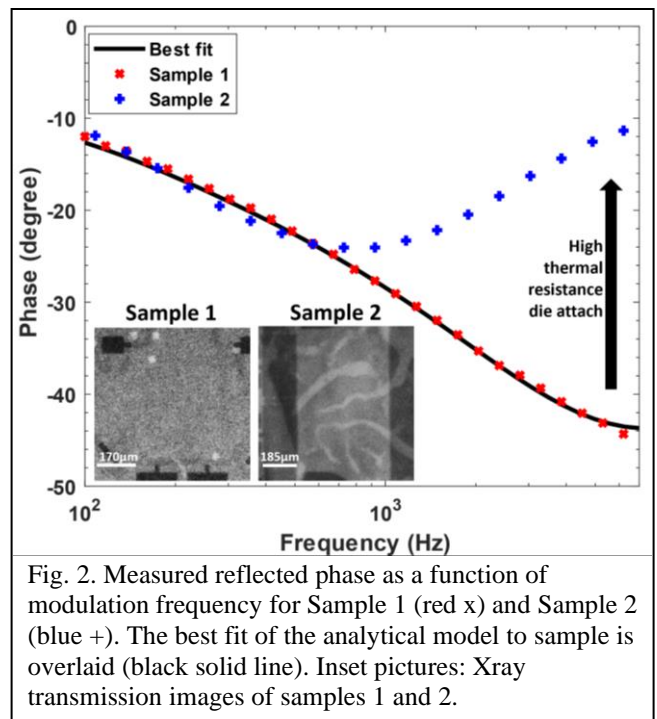


Fig. 2. Measured reflected phase as a function of modulation frequency for Sample 1 (red x) and Sample 2 (blue +). The best fit of the analytical model to sample is overlaid (black solid line). Inset pictures: Xray transmission images of samples 1 and 2.

TABLE I: PROPERTIES OF EACH MATERIAL IN THE DIE ATTACH SAMPLE. THE PROPERTIES INCLUDE: THERMAL CONDUCTIVITY (κ), DENSITY (ρ) AND SPECIFIC HEAT CAPACITY (c_p).

| Material | κ (W/m \cdot K) | ρ (g/cm 3) | c_p (J/g \cdot K) |
|------------|-------------------------------------|---------------------|-----------------------|
| GaN | 156 [7] | 6.15 [8] | 0.490 [9] |
| SiC | 420 [7] | 3.21 [10] | 0.648 [11] |
| Die attach | 72 ± 5 (fitted) ^a | 8.58 [12] | 0.233 [12] |
| Copper | 390 [13] | 8.94 [13] | 0.386 [14] |

^a Fitted effective thermal conductivity

CONCLUSIONS

A novel low-frequency FDTR instrument is demonstrated by successfully measuring the effective thermal conductivity of a die attach layer sandwiched between a die and a flange. In addition, this technique can detect high thermal resistance areas in the die attach layer such as those caused by local voids.

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REFERENCES

- [1] V. R. Manikam & K.Y. Cheong, IEEE Trans. Compon. Packag. Manuf. Technol., Vol. 1, No. 4 (2011).
- [2] W. J. Parker *et al.*, J. Appl. Phys. 32, p. 1679-1684 (1961).
- [3] A. J. Schmidt *et al.*, Rev. Sci. Instrum. 80, 094901 (2009).
- [4] N. Poopakdee *et al.*, Submitted to ACS Appl. Electron December 2021.
- [5] K. Kurabayashi & K. E. Goodson, IEEE Trans. Comp., Packag., Manf. Technol. Part A 21 506-514 (1998).
- [6] J. Yang *et al.*, Rev. Sci. Instrum. 87, 014901 (2016).
- [7] J. W. Pomeroy *et al.*, Microelectronics Reliability 55, pp. 2505-2510 (2015).
- [8] *CRC Handbook of Chemistry and Physics*, 92nd Edition, Edited by W. M. Haynes, CRC Press, Boca Raton, FL. 2011, pp. 4-64.
- [9] M. E. Levinshtein *et al.*, *Properties of Advanced Semiconductor Materials: GaN, AlN, InN, BN, SiC, SiGe*, Wiley & Sons, Inc., New York, pp. 1-30 (2001).
- [10] <http://www.ioffe.ru/SVA/NSM/Semicond/SiC/basic.html>
- [11] R. Wei *et al.*, J. Appl. Phys. 133, 053503 (2013).
- [12] G. Bai, *Low-Temperature Sintering of Nanoscale Silver Paste for Semiconductor Device Interconnection*. Ph. D. Dissertation, Virginia Polytechnic Institute and State University, 2005, pp. 86-87.
- [13] *CRC Handbook of Chemistry and Physics*, 86th Edition, Edited by D. R. Lide, CRC Press, Taylor & Francis Group, Boca Raton, FL. 2005, pp. 2544.
- [14] Y. S. Touloukian & E. H. Buyco, *Thermophysical properties of matter – the TPRC Data Series, Volume 4, Specific Heat – metallic elements and alloys*, (Reannouncement), Data book, 1971: Purdue Univ., Lafayette, IV (United States). Thermophysical and Electronic Properties Information Center.